UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,795	11/07/2000	Stefanos Sidiropoulos	RB1-005US (RA166.P.US)	2457

38489 7590 12/22/2005

SILICON EDGE LAW GROUP, LLP
6601 KOLL CENTER PARKWAY
SUITE 245
PLEASANTON, CA 94566

EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,795	SIDIROPOULOS ET AL.	
	Examiner	Art Unit	
	Edith M. Chang	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *54-62* is/are allowed.

6)☒ Claim(s) *1,2,4-7,9-14,16-25,27-35,37-40,42-44,46-50,52,53 and 63-67* is/are rejected.

7)☒ Claim(s) *3,8,15,26,36,41,45 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050930*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments/Remarks

1. Applicant's arguments filed on September 30, 2005 have been fully considered but they are not persuasive.

Argument: Applicants argue that the signal on node V_{R0} of Perner reference is not a "buffered" voltage.

Response: The "a buffered voltage" is defined in the claim as a produced voltage that is derived at least in part from the common reference voltage by a reference receiver.

The buffers as amplifiers, voltage followers, bipolar or FET transistor, or the common reference voltage being presented on a high-impedance node and the buffered voltage being presented on a low-impedance node, etc. described in the current specification will not be read into the claims, if they are not the limitations recited in the claims. The claims recite a reference receiver, a reference buffer, or a circuit that *receives* the common reference voltage and in response produces a buffered voltage that is derived at least in part from the common reference voltage.

Hence, Perner discloses that the V_{R0} is a buffered voltage derived at least in part from the common reference voltage by the reference receiver/buffer/circuit that *receives* the common reference voltage in Figure 1 *as recited in the claims*.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless —
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-7, 9-13, 16-24, 27-29, 31-33, 37-40, 42-44, 48-49, 52-53, and 63-67 are rejected under 35 U.S.C. 102(b) as being anticipated by Pemer (US 5,818,261).

Regarding **claims 1** & **39,** in Figure 1 Perner teaches a pseudo differential bus driver and receiver for field programmable device, wherein the block 130 contains N precharge device 134s and N pull down device 132s and the block 140 contains N+1 set circuits of elements 142, 144 (NMOS cross point switch, column 3 lines 13-17), 146, and 148 to receive the pseudo differential signals (column 4 lines 13-22). The first set circuit of the first line 142, 144, 146, and 148 (as the reference receiver) receives the reference voltage VREF (the common voltage) on the first line 142 with 146 (as an undistributed reference voltage) to one of the inputs of the first NMOS cross point switch 144 with 146 and 148 and provides a distributed voltage to the gate of each element 144 of the N+1 elements 144s (comprised in N receivers as well) of the block 140, to produce a voltage VRO (as the buffered voltage).

Each of the rest set circuits of elements 142, 144, 146, and 148, and each of the block 150s (as a receiver) receives signals related to 1_1 to I_N on the second line 142 to the N+1 th line 142 to one of the inputs of 144s respectively, wherein the i+1 th set circuit of elements 142, 144, 146, and 148, and the $i^{t}_{s'}$ block 150 (as ^{ith} receiver, i=1 to N, the 2"d to N+1 th set circuits of block 140, column 4 lines 3-12) compose the receivers. The second element 144 with its 146 and 148 and the first block 150 constitute one receiver (1^{st})

receiving an associated signal L10 and the VRO, the third element 144 with its 146 and 148 and the second block 150 constitute one receiver (2^{nd}) receiving an associated signal L20 and the VRO,..., and the N+1 th element 144 with its 146 and 148 and the N^{th} block 150 constitute one receiver (N^{th}) receiving an associated signal LNO and the VRO, to produce the output signal 0 (O_1 to O_N).

Regarding **claims 2** & **40,** in Figure 1 Perner teaches the comparators 156 comparing the associated signal Li0 (i=1 to N) and the VRO to produce the output voltage O.

Regarding **claims 4**, **42** & **67**, in Figure 1 Perner teaches that the VRO proportional to the VREF and is a differential signal (column 4 lines 13-22).

Regarding **claims 5, 43** & **66,** in Figure 1 Perner teaches the VRO presenting the noise of L10 to LNO relative to the V_{REF} on the first line 142 and 146 as shown in the circuit arrangement of Figure 1.

Regarding **claims 6, 7** & **44,** in Figure 1 Perner teaches the first line 142 with 146 (as the common reference voltage) to one of the inputs of the first NMOS cross point switch 144 with 146 and 148 (as the reference receiver) and a gate voltage (as the distributed reference voltage) to the other input of the first NMOS cross point switch 144 that the reference receiver views the relation of (compares) the distributed gate voltage and the common voltage V_{REF} at 144 and is responsive to the distributed gate voltage.

Regarding **claims 9-12**, **20-21, 31-33** & **48-49,** in Figure 1, Pemer teaches the N receivers comprising N set circuits of elements 142, 144, 146 and 148 (the i set circuit, i =1 to N, as the signal buffers) receiving the signals from 132 of I_i to 132 of I_N on lines

142 and in response producing signals L10 to LNO (as the buffered signals) respectively, wherein the LiO (i=1 to N) is subject to a signal capacitance, and the VRO is subject to a reference capacitance which is larger than the signal capacitance as shown in the arrangement of Figure 1 and column 1 lines 45-50 that the longer reference line wiring through more blocks having larger capacitance, hence the reference capacitance 148 of the first set circuit (the reference receiver) is greater than the signal capacitance on the signal line L10; and the receivers of Figure 1 are MOS devices which are source-followers.

Regarding **claims 13** & **24,** in Figure 1, Perrier teaches that the first set circuit with 144 switch having a unity gain.

Regarding **claims 16, 27** & **37**, in Figure 2 and column 4 lines 15-20, Perner discloses the signal receivers 150 comparing the signal voltages V_{SIG} and the VREFREMOTE (the buffered voltage from the reference voltage) to provide two values represented in the OUT. The two values are one is larger than the reference, the other is less than the reference, this is the pseudo differential signaling.

Regarding **claims 17** & **38,** in Figure 1 Perner discloses the VRO the buffered voltage and the reference voltage V_{REF} being subject to similar impedance as the bal

Regarding **claims 18, 28** & **52-53,** in Figure I Perner teaches that the noise is distributed equally between VRO (the buffered voltage) distributed to signal receivers/buffers, and LI 0 to LNO the signal voltages as the layout and structure of the signal receivers 150 and VRO in the logic device 100 to enhance the performance (Abstract).

Regarding **claims 19 & 22-23,** in Figure 1, Perner discloses signal receivers/buffers (each consisting a set circuit of elements 142, 144, 146 & 148 and block 150) receiving associated signal voltages from signal inputs, one of L1O..LNO and the reference voltage from the reference input VRO. The signal receivers/buffers have comparators (element 156 of block 150) comparing the signal voltage LIO (1=0..N) with the reference voltage VRO to produce the output Oi (i=O..N), wherein the input impedance of the element 156 (or the impedance from the LiO) and the impedance of the reference voltage (from the VRO) are similar as two inputs to the signal receiver/buffer 156, and the noise is distributed equally between VRO the buffered voltage and LI 0 to LNO the signal voltages as the layout and structure of the signal receivers 150 and VRO in the receiver end (the second IC) of the logic device 100 of the Figure 1.

Regarding **claims 29, 63 & 65,** in figure 1, Perner discloses the driver (element 130 the first integrated circuit) to transmit the reference voltage on the line 142 to VRO and the signal voltages on signal lines (with elements 132 & 142) to LI0 to LNO, and the receiver end, the second integrated circuit, comprising (elements 150 included in the second IC) its associated pseudo differential signal voltage from signal input, one of LI 0..LNO and the reference voltage from the reference input VRO. The signal receiver (with element 156 in the block 150) compares the signal voltage LIO (1=0..N) with the reference voltage VRO by the element 156 (the comparator) to produce the output Oi (i=O..N). The noise is distributed equally between VRO the buffered voltage and L10 to LNO the signal voltages as the layout and structure of the signal receivers 150 and VRO in the receiver end (the second IC) of the logic device 100 of the Figure 1, wherein

the block 150 is the two-stage signal receiver with the first stage element 156 and the second stage element 154, and with a equalization circuit 152 (column 3 lines 37-41) to reduce/cancel the noise (column 6 lines 25-35).

Regarding claim **64,** in Figure 1 Perner discloses the input impedance of the element 156 (or the impedance from the L10) and the impedance of the reference voltage (from the VRO) are similar as two inputs to the signal receiver/buffer 156.

4. Claims 14, 25, 30, 35, 46-47 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pemer (US 5,8 18,26 1) in view of Boudry (US 5,644,254).

Regarding **claims 14, 25, 30, 35, 46-47** & **50,** in Figure 1 Perner discloses the reference voltage VRO on the reference line/bus and signal voltage L10 on a signal line/bus on the circuit board. It is well know the reference line and signal line bear inductance and capacitance as the characteristic of the impedance, but Perner does not explicitly show the inductance.

However, Boudry teaches the scientific phenomenon in FI G.2 and column 1 lines 45-60, wherein the capacitance and inductance result in a resonant frequency for optimizing impedance. As Perner's pseudo differential bus driver/receiver (element 100) using lines/buses being close to each other to transmit signals, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the Boudry's teaching for the purpose to have matched impedance to reduce the power assumption and provide clear signal (column 1 lines 15-30).

5. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perner (US 5,818,26 1) in view of Sessions (US 5,994,925).

Regarding claim **34,** Perner does not specify the reference buffer as a unit gain Amplifier, however, Sessions teaches a CMOS inverter (as the unit gain amplifier, column 1 lines 14-18) as the receiver buffer. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have the MOS switch 144 of the reference buffer replaced by the CMOS inverter taught by Sessions to receive the reference voltage/signal to produce the VRO for the purpose to provide the accuracy of a differential receiver while reducing power dissipation (column 1 lines 60-63).

Allowable* Subject *Matter

6. Claims 3, 8, 15, 26, 36, 41, 45 and 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims; and overcomes the objections set forth in this office action.

7. Claims 54-62 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest, alone or in a combination, among other things, at least an integrated circuit apparatus and its method of pseudo-differential voltage signaling as a whole, the combination of elements and features, which includes a reference receiver/buffer is a unity gain amplifier to produce a buffered

voltage that represents the difference between an undistributed voltage in part on a common voltage and a distributed voltage received by multiple signal receivers, or the reference receiver/buffer having bandwidth of at least ten times the resonant input frequency, wherein the coupled signal noise introduced in the pseudo-differential voltage signaling is canceled.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay K. Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 14, 2005

KHAI TRAN
PRIMARY EXAMINER